5. The method of Claim 1 wherein the first layer of photoresist and the layer of TiN are removed by a process utilizing fluorine containing gas chemistry at an elevated temperature.

REMARKS

Claims 1 and 3 – 5 are pending in the application and stand rejected. Applicants have not amended the Claims because the Examiner has apparently misread the cited reference. Applicants request that the Examiner withdraw his/her rejection and issue the application.

The Examiner rejected Claim 1 under 35 U.S.C. 102(e) as being anticipated by Xing et al. (U.S. Patent No. 5,880,026). The Examiner stated that:

> Referring to figures 1-3D, Xing et al. teaches a method of manufacturing a semiconductor device, wherein the method comprises: forming a final layer of metal (210, 230, 240, 250) on a layer of interlayer dielectric (270) in the semiconductor device; forming a layer of TiN (205) on the final layer of metal; forming a first layer of photoresist (200) on the layer TiN; patterning and developing the first layer of photoresist exposing portions of the layer of TiN (see figure 2A and related text); etching holes in the layer of TiN and the final layer of metal exposing portion of interlayer, wherein metal structures are formed; removing the first layer of photoresist (see figure 2B and related text); removing remaining portions of the layer of TiN (see figure 2C) **[THE EXAMINER IS IN ERROR—THE REMAINING PORTIONS OF TiN ARE NOT REMOVED, THE LAYERS (UNNUMBERED IN FIGURE 2C) OVER STRUCTURES 240 ARE TiN AND HAVE NOT BEEN REMOVED—NOTE THAT THE UNNUMBERED LAYERS, WHICH ARE TiN, REMAIN IN FIGURE 2D]**; and forming a blanket layer of interlayer dielectric on the surface of the semiconductor device (280).

In view of the fact the Examiner misinterpreted the cited reference (Xing et al.), the rejection under 35 U.S.C. §102(e) is in error and must be withdrawn. In addition, as will be discussed below, any conclusion of obviousness is also in error.

The Examiner rejected Claims 1, 3-5 under 35. U.S.C. §103(a) as being unpatentable over Xing et al. (U.S. Patent No. 5,880,026) in view of the Admitted Prior Art). The Examiner stated:

> Referring to figures 1 – 3D, Xing et al. teaches a method of manufacturing a semiconductor device, wherein the method comprises: forming a final layer of metal (210, 230, 240, 250) on a layer of interlayer dielectric (270) in the semiconductor device; forming a layer of TiN (205) on the final layer of metal; forming a first layer of photoresist (200) on the layer of TiN; patterning and developing the first layer of photoresist exposing portions of the layer of TiN (see figure 2A and related text); etching holes in the layer of TiN and final layer of metal exposing portion of interlayer dielectric, wherein metal structures are formed; removing the first layer of photoresist (see figure 2B and related text); removing remaining portions of the layer of TiN (see figure 2C) **[AS SHOWN AND DISCUSSED ABOVE,**

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THIS IS INCORRECT, THE REMAINING PORTIONS OF THE LAYER OF TiN IS NOT REMOVED]; and forming a blanket layer of interlayer dielectric on the surface of the semiconductor device (280).

In view of the discussion above and because the Examiner misinterpreted Xing et al., this statement by the Examiner is irrelevant.

The Examiner admitted, however, that:

> However, the reference does not teach depositing a second photoresist layer, patterning and etching the layer of photoresist and blanket layer to exposed the metal layer, etching the photoresist layer and TiN layer by using fluorine containing gas chemistry at an elevated temperature.

In view of the discussion above concerning the error by the Examiner and the fact that more of the claimed invention is not shown, this is further evidence that the rejection must be withdrawn.

The Examiner continued:

> Referring to figures 1a-1I, the Admitted Prior Art teaches a method of manufacturing a semiconductor device comprises: forming a final metal layer (104) over the interlayer dielectric (102), forming a TiN layer (106) over the metal layer, forming a layer of photoresist (108) over the TiN layer, patterning and developing the first layer of photoresist exposing portions of the TiN layer, etching in the layer of TiN and the final layer of metal exposing portions of the interlay dielectric layer, removing the first layer of photoresist and the layer of TiN, depositing a blanket layer (114), forming a second photoresist layer (116) on the blanket layer of interlayer dielectric; patterning and developing the second layer of the photoresist layer exposing portions of blanket layer of interlayer dielectric overlying metal structures; and etching the exposed portion of the blanket layer of interlayer dielectric down to the metal structures, removing the second layer of the photoresist (see figures 1a-1I of the Admitted Prior art and related text).

The Examiner then concluded:

> Therefore, it would have been obvious to one of ordinary skill in the requisite art at the time the invention was made would form a second photoresist layer, patterning and etching the layer of photoresist and blanket layer to expose the metal layer as taught by the Admitted Prior art in process of Xing et al. because the technique is known in manufacturing a semiconductor device.

Initially, Applicants wish to make it clear that the Applicants are not interested in any way as to the unsubstantiated opinion of the Examiner. If the Examiner wishes to make a

determination of obviousness, the Examiner is required to point out in the cited prior art where it is disclosed, taught or suggested to make the claimed combination.

Applicants have pointed out that the Examiner has made an error in the interpretation of Xing et al. and as even more apparent, no matter how the disclosure and teaching of Xing et al. is combined with what the Examiner has termed the "Admitted Prior Art" the claimed invention is not disclosed, taught or suggested.

The Examiner also stated:

> The examiner takes Official Notice that the embodiment described in claim 5 would have been obvious to skilled worker in the art at the time the invention was made because determining the optimum material for etching the layer only involved routine skill in the art (see MPEP 2144.03).

Applicants submit that this is complete utter nonsense. Nowhere in the application is stated or suggested that the material used for etching was the "optimum" material. The inventors have invented a way to "simultaneously remove photoresist and the layer of TiN" using a particular material. If the Examiner wishes to reject Claim 5, the Examiner is required to find a reference that either uses the claimed material or suggests the use of the claimed material.

The Examiner is invited to point out exactly where in the cited prior art there is a disclosure, teaching or suggestion for the formation of the combination as taught and claimed in the present invention. Again, Applicant submits that there is none!!!

APPLICANT SUBMITS THAT THE ROLE OF EXAMINER IS NOT TO "SUBJECTIVELY" CONCLUDE THAT SOMETHING IS OBVIOUS WITHOUT BEING ABLE TO SHOW WHERE IN THE PRIOR ART THERE IS AT LEAST A SUGGESTION TO MAKE THE COMBINATION.

Here the Examiner has found disparate and disjointed elements in more than one references some of which do not resemble the elements in the present invention and has made the unwarranted conclusion that the combination as taught and claimed in the present invention is "obvious." Applicant submits that the conclusion is nonsense.

The semiconductor manufacturing industry expends many millions of dollars in research and development to find improvements in the manufacture of semiconductors and how the semiconductor devices function. Each such improvement comes at the expense of time and money by the semiconductor manufacturer and after many hours of testing and evaluation. The semiconductor

manufacturers certainly do not expend all of these resources needlessly on "obvious" inventions. For an Examiner to conclude, without any objective evidence, that something "would be obvious" is ludicrous and is considered so by the semiconductor industry. In addition, for the Examiner to make a conclusion based upon a mistaken interpretation of one of the cited references is completely ludicrous.

The judicially established standard for a finding of obviousness is that: "There must be some reason suggestion, or motivation found in the prior art whereby a person of ordinary skill in the field of the invention would make the combination. That knowledge cannot come from the applicant's invention itself. In re Oetiker, 977 F.2d 1443, 1447 (Fed. Cir. 1992) *citing* Diverstech Corp. v. Century Steps, Inc. 850 F.2d 675, 678-9 (Fed. Cir. 1988).

Furthermore, the Federal Circuit has made it clear that: "The PTO has the burden under section 103 to establish a *prima facie* case of obviousness. *See In re Piasecki,* 745 F.2d 1468, 1471-1472 (Fed. Cir. 1984). It can satisfy this burden only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references. In re Fine, 837 F. 2d 1071, 1074, 5 USPQ 2d 1596, 1598 (Fed. Cir. 1988) *citing* In re Lalu, 747 F. 2d 703, 705 (Fed. Cir. 1984).

Obviousness is tested by "what the combined teachings of the references would have suggested to those of ordinary skill in the art." In re Keller, 642 F.2d 413, 425 (CCPA 1981). **But it "cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching or suggestion supporting the combination."** ACS Hosp sys. [Inc. v. Montefiore Hosp., 732 F.2d 1572, 1577 (Fed. Cir. 1984). [emphasis added] **And "teachings of references can be combined *only* if there is some suggestion or incentive to do so."** In Re Fine, 837 F.2d 1071, 1075 (Fed. Cir. 1988). [emphasis added]

The critical inquiry is whether "there is something in the prior art **as a whole** *to suggest* the desirability, and thus the obviousness of making the combination." Fromson v. Advance Offset Plate, Inc., 755 F.2d 1549, 1556 (Fed. Cir. 1985) *quoting* Lindemann Maschinenfabric GMBH v. American Hoist & Derrick Co., 730 F.2d 1453 (Fed. Cir 1984).

It is apparent that the Examiner has not complied with the above-quoted standards established mainly by the Federal Circuit. The question is WHY hasn't the Examiner complied with standards and why doesn't the Applicant have the right to expect that his application will be examined by the

standards established by the Federal Circuit. Applicant is not satisfied that the present application has been examined based upon unsubstantiated opinions of the Examiner.

In view of the above, Applicants submit that the application is in condition for allowance and request an early allowance.

Respectfully submitted,

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I certify that this document is being deposited on 11/17/00 with the U.S. Postal Service as first class mail under 37 C.F.R. §1.8 addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231

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